CLAIMS

WHAT IS CLAIMED IS:

1. A method of fabricating an array of pores, comprising the steps of:

applying a first layer of a first material onto a substrate;

removing a portion of said first layer of said first material to define an upper surface with generally vertical surfaces extending therefrom to a lower surface in said first layer of said first material;

applying a fixed layer of a second material onto said generally vertical surfaces of said first layer of said first material, said fixed layer of said second material having a first thickness;

applying a second layer of said first material onto said fixed layer of said second material; and

removing said fixed layer of said second material to define said array of pores in said first material layers.

2. The method of claim 1, wherein said pores have a minimum lateral dimension ranging from approximately 50 to 500 Angstroms.

3. The method of claim 1, wherein said pores have a cross sectional area greater than or equal to said first thickness of said layer of said second material squared.

4. The method of claim 1, wherein said pores have a minimum lateral dimension ranging from approximately 50 to 500 Angstroms; and wherein said pores have a cross sectional area greater than or equal to said first thickness of said layer of said second material squared.

5. The method of claim 1, wherein said upper surface is generally horizontal and includes a horizontal surface which is generally cross shaped.

6. The method of claim 5, wherein said cross shaped horizontal upper surface includes a pair of arms extending relative to a central point.

7. The method of claim 6, wherein said arms of said cross shaped horizontal upper surface range in length from about .5 to 1. microns.

8. The method of claim 1, wherein said upper surface is surrounded by a recess defined in part by said lower surface.

9. The method of claim 8, wherein said upper surface includes a plurality of arms extending laterally relative to a generally central location.

10. The method of claim 1, wherein said first material is comprised of silicon nitride.

11. The method of claim 1, wherein said second material is comprised of silicon dioxide.

12. The method of claim 1, wherein said first material is comprised of silicon nitride and wherein said second material is comprised of silicon dioxide.

13. An array of pores fabricated by a process comprising the steps of:

applying a first layer of a first material onto a substrate;

removing a portion of said first layer of said first material to define an upper surface with generally vertical surfaces extending therefrom to a lower surface in said first layer of said first material;

applying a fixed layer of a second material onto said generally vertical surfaces of said first layer of said first material, said fixed layer of said second material having a first thickness;

applying a second layer of said first material onto said fixed layer of said second material; and

removing said fixed layer of said second material to define said array of pores in said first material layers.

14. The array of pores of claim 13, wherein said pores have a minimum lateral dimension ranging from approximately 50 to 500 Angstroms.

15. The array of pores of claim 13, wherein said pores have a cross sectional area greater than or equal to said first thickness of said layer of said second material squared.

16. The array of pores of claim 13, wherein said pores have a minimum lateral dimension ranging from approximately 50 to 500 Angstroms; and wherein said pores have a cross

sectional area greater than or equal to said first thickness of said layer of said second material squared.

17. The array of pores of claim 13, wherein said upper surface is generally horizontal and includes a horizontal surface which is generally cross shaped.

18. The array of pores of claim 17, wherein said cross shaped horizontal upper surface includes a pair of arms extending relative to a central point.

19. The array of pores of claim 18, wherein said arms of said cross shaped horizontal upper surface range in length from about .5 to 1 micron.

20. The array of pores of claim 13, wherein said upper surface is surrounded by a recess defined in part by said lower surface.

21. The array of pores of claim 20, wherein said upper surface includes a plurality of arms extending laterally relative to a generally central location.

22. The array of pores of claim 13, wherein said first material is comprised of silicon nitride.

23. The array of pores of claim 13, wherein said second material is comprised of silicon dioxide.

24. The array of pores of claim 13, wherein said first material is comprised of silicon nitride and wherein said second material is comprised of silicon dioxide.

25. A chalcogenide memory cell, comprising:

an upper electrode;

a lower electrode;

a dielectric layer positioned between said upper and lower electrodes and including an opening defining a pore;

a chalcogenide element within said pore, said chalcogenide element electrically coupled to said upper and lower electrodes;

wherein said pore has a minimum lateral dimension ranging from about 50 to 500 Angstroms.

26. The chalcogenide memory cell of claim 25, wherein said pore has an L shaped cross section.

27. A method of fabricating an array of chalcogenide memory cells, comprising the steps of:

applying a first layer of dieleetric material onto a substrate that includes an array of conductive regions;

removing a portion of said first layer of said dielectric material to define an upper surface with generally vertical surfaces extending therefrom to a lower surface in said first layer of said dielectric material;

applying a fixed layer of a second material onto said generally vertical surfaces of said first layer of said dielectric material, said fixed layer of said second material having a first thickness;

applying a second layer of said dielectric material onto said fixed layer of said second material;

removing said fixed layer of said second material to define an array of pores in said dielectric material layers, said array of pores generally vertically aligned with said array of conductive regions of said substrate; and

providing a chalcogenide memory cell at each of said pores by the steps comprising:

applying a layer of chalcogenide material onto a region of said dielectric material layer generally centered at said pore, said layer of chalcogenide material extending into said pore; and

applying a layer of conductive material onto said chalcogenide layer.

28. The method of claim 27, wherein said pores have a minimum lateral dimension ranging from approximately 50 to 500 Angstroms.

29. The method of claim 27, wherein said pores have a cross sectional area greater than or equal to said first thickness of said layer of said second material squared.

30. The method of claim 27, wherein said pores have a minimum lateral dimension ranging from approximately 50 to 500 Angstroms; and wherein said pores have a cross sectional area greater than or equal to said first thickness of said layer of said second material squared.

31. The method of claim 27, wherein said upper surface is generally horizontal and includes a horizontal surface which is generally cross shaped.

32. The method of claim 31, wherein said cross shaped horizontal upper surface includes a pair of arms extending relative to a central point.

33. The method of claim 32, wherein said arms of said cross shaped horizontal upper surface range in length from about .5 to 1 micron.

34. The method of claim 27, wherein said upper surface is surrounded by a recess defined in part by said lower surface.

35. The method of claim 34, wherein said upper surface includes a plurality of arms extending laterally relative to a generally central location.

36. An array of chalcogenide memory cells, comprising:

a plurality of chalcogenide memory cells positioned in a generally common plane,

each said chalcogenide memory cell including:

an upper electrode;

a lower electrode;

a dielectric layer positioned between said upper and lower electrodes and including an opening defining a pore;

a chalcogenide element within said pore, said chalcogenide element electrically coupled to said upper and lower electrodes;

wherein pores of adjacent chalcogenide memory cells are spaced apart by a distance ranging from about .25 to .5 microns.

37. The array of claim 36, wherein a minimum lateral dimension of said pores ranges from about 50 to 500 Angstroms.

38. The array of claim 36, wherein each of said pores have an L shaped cross section.